ARCOS - Arcetri correlator spectrometer
Clock generation module

G.Comoretto[1], G. Tuccari[2], G. Nicotra[2], S. Buttaccio[2]

July 1993

1) Osservatorio Astrofisico di Arcetri
2) C.N.R. Istituto di Radioastronomia

Arcetri Technical Report N° **3/1993**

Abstract

The clock and sequence generation module for the Arcetri correlator spectrometer (ARCOS) is presented. The module generates: the clock signals for all the digital logic in the instrument, the sequence of signals used for timing the integration frame, a set of test pattern for diagnostic purposes and two interrupt signals for the control CPU. All signals are derived by a master clock oscillator at 160 MHz. The module is fully programmable by the instrument control computer via the VME control bus. Most of the module logic is implemented using three Xilinx programmable gate arrays.

1 Introduction

The ARcetri COrrelation Spectrometer (ARCOS), is a general purpose spectrometer for cm and mm wavelength thet is currently being built by the Arcetri Radioastronomy group. Two copies of the instrument will be built, that will be used mainly in the Medicina and Noto radiotelescopes.

The principal characteristics of the instrument (described in Comoretto et al, 1991 [4]) are:

- Maximum instantaneous bandwidth of 160 MHz
- Up to 8 independent channels
- Up to 2048 spectral channels, that can be split among the channels used (expandable to 4096).
- Minimum bandwidth of 0.3 MHz, and spectral resolution of 160 Hz

The instrument requires several clock signals, that must be coherently generated. Some of these signals must be programmable in frequency.

Each correlation card requires a correlation clock, used in the multiplier, and a shift clock, that determines the bandwith of the correlator section. The correlator clock is fixed at 40 MHz, while the shift clck can be varied to accomodate for different bandwidths. Since up to 4 cards can be present in the instrument, 4 clock signals of each type are required.

The correlation cards used have a limited integration memory, and must be read at intervals not greater than 10 ms. The integration must be stopped, the integration memory transferred in a on-board buffer memory, the integrators cleared and the integration then resumed. The sequence must be accurately timed, but is sufficently simple to be performed by a dedicated logic circuit.

The correlator requires some test signals, to exercise the instrument and for diagnostic purposes. The present design includes a square wave and a pseudo random bit sequence, both of them with programmable frequency.

All these signals are generated in a clock generation module (clock card). The signals are all derived from a master clock at 160 MHz. The module communicates with the control computer using a VME standard interface. The control computer must be interrupted at periodic intervals during the observation, at the end of each integration frame to read the intergration buffers and at periodic intervals to read the total power meters. The clock module therefore includes a VME interrupter circuitry. The module generates also a few other ancillary clock signals, required in the sampler card.

The VME interface used is standard interface developed by the staff of the Noto radiotelescope. It is not described here, and will be the subject of a separate report.

2 General description

The clock generation board must provides timing signals for the whole instrument, i.e. sampler clock for the samplers, shift and multiplication clock for the correlators, and the integration syncronization signals for the correlator boards. In addition, a test pattern is generated to exercise the boards and for debugging purposes.

The general structure of the board is shown in the schematics in fig. 1, while the board layout is shown in fig. 2. A master clock, at 160 MHz, generates the main clock signal, from which all other signals are derived. A 160 MHz 0 dBm ECL square wave is generated by a temperature-controlled crystal oscillator (TCXO). The ECL signal is buffered by a 10H123 to generate the two 160 MHz clock signals for the sampler cards.

This signal is thus divided by 4 in a 10H016, and translated to TTL logic levels by the 10H125. The 40 MHz signal, buffered by 6 50Ω line drivers, is sent to the 2 sampler cards, where it is used to resample the input signal at the final sampling frequency, and to the 4 correlator cards, for the correlation timing (correlator board CLADD signal). The correlation is always done at 40 MHz, irrispective of the shift frequency.

The 40 MHz signal is also fed to a XC2064 Xilinx gate array, (citexilinx:a that generates the 8 possible shift frequencies, and select the appropriate one for each correlation card (correlator board CLSR signal). The possible frequencies range from 312.5 KHz to 40 MHz, in binary steps, and can be set independently for each card.

The gate array also generates a test pattern for debug purposes. The pattern can be chosen between a square wave 2 bit long and a pseudo random sequence 2047 bit long. The period of the test pattern (the length of each "bit" in the sequence) can be chosen independently from the shift frequencies.

A 10 MHz signal from the first gate array is fed into a second gate array, that generates all the timing signals for the correlation cards, i.e. LDRAM, INHADD, RESET. During an integration, the card generates periodically the appropriate sequence of these signals at a selectable interval, to terminate the integration frame, load it in the on-chip buffers, restart the next frame, and interrupt the processor to read the chips. The frame duration can be set from

1 to 31 ms, in 1ms steps.

The gate array generates also a pulse with a selectable period (usually 100 ms) and a duration of 100 ns, to be used as a syncronization signal in the total power monitor circuit. This pulse may also be used to generate an interrupt, to trigger the total power monitor routine.

The two gate arrays are interfaced to the VME bus, and each one contains a 16 bit read/write register. The VME interface has been developed by the Noto group of the CNR, Istituto di Radioastronomia [7], as a single custom gate array. It contains the address selection logic for up to 8 on-board registers (2 used in this board), and a general purpose interrupter, with up to 4 independent interrupts (2 used in the module).

Two signals, with fixed periods of 10 MHz and 312 KHz, are carried to the output connector to e used as a reference frequency for the sampler threshold control PLL's and to generate the sampler PLL's initialization signals in the sampler boards.

3 Backplane and VME interface

The clock module is connected to the instrumento control computer using a standard A16-D16 VME interface, and to the other modules in the instrument using a dedicated connector.

The module uses connector J1 (a standard 603-2-IEC-C096M 96 pole VME-type connector) for the VME interface. The interface is implemented using a custom gate array, plus two ALS645 bidirectonal buffers and two 7406 open collector drivers for electric compliance to the VME bus specifications.

The gate array decodes the A01-A15 address lines and AM0-AM5 address modifiers, and generates the proper handshaking signals according to the VME-bus specifications. It includes also a complete interrupt, with programmable interrupt level and vector address. The VME interface is not described in detail here, since it is a general purpose interface common to all the boards in the instrument.

The board responds to the address modifier codes 0x2d (Short supervisor access) and 0x29 (Short non-privileged access). The upper 8 bits of the address decoded (A08-A15) are selectable using two hexadecimal rotary switches. U19 specifies the MSB of the address part, The board thus responds to a block of 256 consecutive addresses, but only the first 9 words (18 bytes) are accessible. Strobes for the first 8 words are available form the gate array, while the 9^{th} word controls the interrupt usage. The board responds also only to word accesses (16 bits), and not to separate byte accesses. In the clock module, only 3 words are used. These three registers are listed in table 1.

Two dip switches are used to specify the delay for the DTACK signal. This delay is specified by the dip switches S1-1 and S1-2, according the to the table in 2.

Address	Register
0x00	Shift clock control register
0x02	Timing generation control register
0x10	Interrupt control register

Table 1: Clock module control registers

SW 1 Setting 1 2	DTACK delay
0 0	200 ns
0 1	400 ns
1 0	600 ns
1 1	800 ns

Table 2: DTACK delay setting

The shift clock and timing generation control registers are described in detail resp. in tables 5 and 7, and in the following chapters The interrupt control register is used to select the interrupt priority level (and thus the interrupt line used), and the interrupt vector. It is also used to globally disable the interrupts in the board.

The interrupt vector is a 8-bit quantity that is supplied to the control computer by the interrupt logic as a part of the interrupt acknowledge cycle. It is used to identify the interrupter source, and thus to select the appropriate interrupt service routine. It is usually set by the interrupt initialization routine. The board supports up to 4 independent interrupts, and therefore can generate up to 4 different vectors. The interrupt vector is thus generated using 6 bits supplied by the control computer in the interrupt control register, and coding the interrupter source in the two least significant bits of the vector. For example, if the vector specified in the control register is 0x60, an interrupt received on the interrupt line IR1 generates an interrupt vector of 0x61. All interrupts occur on the same interrupt line, and are internally prioritized with interrupt line IR3 having the highest priority. The only interrupt lines used are IR0, used to signal the end of an integration frame, and IR1, for the general-purpose periodic interrupt. Lines IR0–IR3 are active low, level sensitive, with an internal pullup resistor.

The format of the interrupt control register is shown in tab. 3. One bit of this word is not used by the interrupt logic, and is available on pin B7 of the gate array.

The signals generated by the clock module are carried to the other modues

Bit	Function
0	Global interrupt enable
1	Auxiliary bit
2–7	Interrupt vector bits 2–7
8–10	Interrupt level
11–15	Not used

Table 3: Bit assignment for interrupt control register

in the system using connector J2. This connector is a standard, male connector DIN41612 24+8 (24 pins and 8 coaxial contacts). The eight coaxial contacts are used for the 160 MHz and 40 MHz clock signals to the correlator and sampler boards. All the other signals are routed using the conventional contacts. The connector pinout is listed in tab. 4.

4 Shift clock gate array

The shift clock for the four correlator boards, the test pattern and most of the periodic clocks are generated in a XC2064 programmable gate array (U16 in fig. 1). The XC2064 is a user-configurable device composed of 64 macrocells, each containing combinatory logic and a flip-flop, and a set of input-output blocks, containing a flip-flop and a three state buffer. These cells can be connected in an arbitrary way, [5].

The gate array equivalent circuit is shown in fig. 3. The circuit is drawn using the Xilinx Orcad interface. Details on the implementation of the Xilinx macros can be found in the associated literature [6].

The gate array generates all the eight possible shift frequencies, by successive binary divisions, and selects them for the four correlation cards. The general layout of the chip is shown in fig. 4. The input register uses the 16 upper I/O pins and their associated flip-flops, and can be read back by the processor. The bit assignment in this register is shown in tab. 5.

The control register is accessed when the SEL input line of the gate array is low. If WRITE is low, data on the lines P0–P15 are strobed in the control register during the rising edge of SEL. If WRITE is high, data in the control register is placed on the bus for all the duration of the SEL low signal. When SEL is high, the P0–P15 lines are in a high impedance status.

The divider has been implemented as a 7 bit syncronous binary divider. To allow the high counting speed of 40 MHz, the layout of each divider has been accurately designed, using almost only direct interconnects between adjacent blocks. Since the propagation delay through 7 logic blocks was too long, the first 4 bits form an independent counter, and its terminal count signal has been

Pin number	Column A	Column B	Column C
2	CLADD Ch. 0 (coax)		
5	CLADD Ch. 1 (coax)		
8	CLADD Ch. 2 (coax)		
11	CLADD Ch. 3 (coax)		
13	CLSR Ch. 0	GND	LDRAM
14	CLSR Ch. 1	GND	RESET
15	CLSR Ch. 2	GND	STATUS
16	CLSR Ch. 3	GND	INHADD
17	Tot. pow. pulse	GND	Test sig magn.
18	10 MHz ref.	GND	Test sig sign
19	-12 V supply	GND	-12 V supply
20	+15V supply	GND	312.5 KHz
22	40 MHz sampl. 0 (coax)		
25	40 MHz sampl. 1 (coax)		
28	160 MHz sampl. 0 (coax)		
31	160 MHz sampl. 1 (coax)		

Table 4: Pin assignment for connector J2

Bit	Function
0–2	Clock selection for card 0
3–5	Clock selection for card 1
6–8	Clock selection for card 2
9–11	Clock selection for card 3
12–14	Clock selection for test signal 0
15	Test signal type: 0=square 1=noise

Bit	Function
0	312.5 KHz
1	625 KHz
2	1.25 MHz
3	2.5 MHz
4	5 MHz
5	10 MHz
6	20 MHz
7	40 MHz

Table 5: Bit assignment for control register in clock LCA (left) and frequency codes (right)

resyncronized to the 40 MHz clock (and thus delayed by a clock cycle). The delayed TC signal is then used to enable the final 3 counter stages. In this way the counter operates in a "pipelined" mode. The first 4 bits are always a clock cycle ahead with respect to the last 3, but are resyncronized by four dedicated flip-flops.

The eight clocks are fed via long horizontali lines to five 8-to-1 selectors. These selectors also use extensively direct interconnections between vertically adjacent blocks, for minimum skew in switching from one clock frequency to the other. Four selectors drive the four shift clock outputs, and the fifth is used to generate the test signal.

The chip can generate two kind of test signals. When bit 15 of the control register is set to 0, the test clock drives a toggle flip flop to generate a square wave with frequency between 156 KHz and 20 MHz. The square wave is applied only to the sign bit, and the magnitude bit is always 1. The flip flop used is the last one of the test pattern generation shift register (U135 in fig. 3).

When bit 15 is set to 1, both the sign and the magnitude bits are generated by a pseudorandom noise generator, composed by a 11 stage shiftregister. The correlation function of the generated bit stream is known, and can e compared to the correlator output. Since the signal has an almost perfectly flat spectrum, however, the correlator is tested in a much more realistic condition than with a square wave.

The test clock can be varied independently from the shift clock of any correlation board. In this way, the frequency (or the bandwidth, for the test pattern) of the test signal can be varied under program control.

The timing of the correlation clock signal is very critical. Therefore it has been finely tuned, choosing different internal routes in the PGA, to achieve constant timings both between different shift clock signals and when the clock frequency is varied. For the correlation card to operate correctly, the active edge of the 40 MHz clock (CLADD) must be syncronous with that of the shift clock (CLSR). Note however that the active edge at the board input is the **FALLING** one, because of the odd number of inversions that are present in the buffer chain of these signals in the correlation board.

The actual timings measured for CLSR at the outputs of a XC2064, for programmed device, are reported in tab. 4.

5 Timing generation

The second gate array generates all the timing necessary to correctly execute an integration. The correlation cards have a limited integration capability of about 12 ms, and an integration must therefore be broken in small sections, each not longer than about 10 ms, called *integration frames.*

Each frame is timed by driving in the appropriate sequence the signals RESET, INHAD, and LDRAM, in order to:

Frequency	Ch 0 clock	Ch 1 clock	Ch 2 clock	Ch 3 clock	Test clock	Test data
312.5 KHz	+0.5	-0.5	-1.0	+1.0	-0.5	+14
625 KHz	+0.5	-1.0	-2.0	+1.0	-1.0	+14
1.25 MHz	+0.5	-0.5	-1.5	+1.0	-0.5	+14
2.5 MHz	+0.5	-1.0	-1.5	+1.0	-1.0	+14
5 MHz	+1.0	-0.5	-0.5	+1.0	+0.5	+14
10 MHz	+1.0	-0.5	-1.0	+1.0	-0.5	+14
20 MHz	+0.5	-1.5	-1.5	+1.0	-0.5	+14
40 MHz	+1.0	-1.5	-1.5	+1.0	-0.5	+14

Table 6: Measured delays for the signals produced in the test chip

1. clear the integrator buffers in the correlator chips
2. start the integration for a definite amount of time
3. stop the integration
4. load the integration results in the on-chip buffers
5. generate an interrupt to the control computer, to start the results readout routine

The cycle composing one frame is then repeated as many times as necessary to complete the integration period.

The timing logic must therefore generate the above signals in the correct timing sequence, and handle correctly the transition from the operating mode of the instrument, when frames are observed in a continuous sequence, to the standby mode, when all the activity is stopped.

The layout of the chip is shown in fig. 5. The schematic equivalent of the circuit is shown in figg. 6.1–6.4.

The timing diagram for the correlation signals is shown in fig. 7.

The chip operates from a 10 MHz clock generated by the shift clock gate array. The basic timing unit is therefore 100 ns. This clock is first divided by 10^4, to generate a 1 KHz pulse. This pulse is counted by a programmable downcounter, to generate a frame length from 1 to 31 ms (fig. 6.3). At the end of this period, a start frame signal is generated, and is propagated in a 8-stage shiftregister to generate all the other signals (fig. 6.4). Each stage output is active for a 100 ns interval, and is named P0–P7. The INHADD signal goes true at P0, and is reset at the beginning of P7. The LDRAM signal is activated during P4, and the RESET signal during P6. The correlation chip specifications require that the LDRAM signal is asserted after at least 5 CLADD cycles plus

100 ns (for a total of 225 ns at 40 MHz). The timing sequence generated by the XC2064 gives a safe margin of 400 ns.

At the begining of P7, the interrupt filp flop is set, driving high the INT0 pin. The VME interrupt logic is part of the VME interface, and responds to this signal generating an interrupt on the bus, if the corresponding interrupt is enabled. When the CPU services the interrupt, it clears the interrupt flip flop by raising bit 0 of the LCA control register. If this last bit is set, interrupts are effectively disabled.

Note that the signals INHADD and LDRAM are negative true, i.e. are active when low. These signals are inverted in the correlation board, and the corresponding signals at the chip input are active true. Moreover, the INHADD signal is delayed a CLRS period in the correlation card. Since this delay would be variable, and potentially very long in our correlator, the syncronization flip-flop has been removed from the correlation boards.

Integration is started and stopped using the START INTEGRATION bit (bit 7) in the control word. Integration is enabled when this bit is set, and disabled when it is clear.

When the bit is set, INHADd os held high, but the sequence logic is enabled. At the next frame boundary (START CYCLE signal), a normal cycle (including the unnecessary signal LDRAM) is generated, correlation chips are cleared, INHADD is released, and the CPU is interrupted a first time to signal that integration is actually started.

When START INTEGRATION is cleared, the current frame is completed, the CPU is interrupted a last time, and the INHADD line is not released as usual. The frame generation logic continues to produce START CYCLE signal at regular intervals, but they are ignored as long as START INTEGRATION is low. As long as START INTEGRATION bit is clear, INHADD is held high, stopping the inegration logic on the correlation chips.

The chip generates a second timing signal, with a period selectable between 50 and 1000 ms. This signal, that lasts one cycle time (100 ns), can be used to syncronize the total power integrators on the samplers. This signal also generaters an interrupt, that is output on pin INT1, and that is enabled setting the correct enabling bits in the interrupt controller. It is cleared by the interrupt service routine rising bit 1 of the LCA control register.

The LCA is controlled by a 16 bit read-write register, accessed in the same way than for the clock LCA. The bit assignment in this register is shown in table 7.

The global chip reset clears all counters on the LCA, thus providing a good way to syncronize the chip on the CPU clock.

The STATUS line selects the STATUS register on the correlation chips. It must be set before programming these chips, and cleared before reading the integration results.

The RESET, LDRAM and INHADD lines are OR-ed with the corresponding signals generated by the LCA. They are normally cleared, and may be set

Bit	Function
0	Frame interrupt clear
1	Timer interrupt clear
2	STATUS control line
3	RESET control line
4	LDRAM control line
5	INHADD control line
6	INTERRUPT signal (read only)
7	Start integration
8–9	Pulse period (50, 100, 500, 1000 ms)
10–14	frame length (ms)
15	Global chip reset

Table 7: Bit assignment for control register in the timing LCA

for debugging purposes. INHADD is normally set, since in standby mode the INHADD line is normally high, and is driven low to allow the correlation chips to integrate.

The pulse period bits select one of four periods for the periodic pulse generated by the LCA. This signal is useful to syncronize total power integrators in the system. The period can be 50, 100, 500 or 1000 ms, resp. selecting the two bits to 00, 01, 10 and 11.

The frame length can be programmed from 1 to 32 ms, in step of 1 ms, by writing (frame length -1) in bits 10–14 of the control register. It is advisable to select a frame length that evenly divide 1 second, so that cycles occur at predictable times. Typical frame length is 20 ms, or 10 ms for very short integrations. When the register is first loaded, the next cycle is completed, and the successive cycle ends after $(N + 2)$ ms. If the frame length is set to zero, the frame generation logic is stopped.

In fig. 7d, the timing of the frame length counter is shown. The counter length register is initially reset to zero, and thus the counter is always trapped in the state 0, with the line CYCLE_TC always asserted. When the frame length counter is loaded with the value 3, the counter begins operation, counting down from 3 to 0. The start cycle sygnal is asserted a first time when the counter begins to operate. It is therefore advisable not to enable integrations before loading the frame length value.

References

[1] A. Bos (1989): *The N.F.R.A. Correlator Chip,* NFRA Internal Technical Report 176

[2] A. Bos (1989): *A General Purpose Correlator Board: Functional Description,* NFRA Internal Technical Report 178

[3] R.P. Millenaar, S. Zwier and A. Bos (1990): *The General Purpose Correlator Board: Hardware description,* NFRA Note 544

[4] G. Comoretto, M. Catarzi, M. Felli, F. Palagi, G. Tofani (1990): *Basic design for a 2048 channel autocorrelator based on the NFRA chip,* Arcetri internal report n. 9/90

[5] *The programmable Gate Array Design Handbook.* Xilinx inc, P/N 0010023 (1986)

[6] *Xact Orcad interface User Guide*, Xilinx Inc. P/N 0400990-01 (1993)

[7] L. Tuccari , S. Buttaccio , G. Comoretto, G. Nicotra, L. Nicotra: *A General purpose VME Server Interface*, IRA-CNR techincal report, in preparation (1993).

Figure captions

Contents