

# Design of a FIR filter using a FPGA

G. Comoretto<sup>1</sup>

<sup>1</sup>Osservatorio Astrofisico di Arcetri

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## **Abstract**

*A modification of the filter design described in Arcetri Technical Report N° 5/2002 is presented. The overall structure is similar, but the the digital local oscillator is moved after the first filter and after the frequency decimation. With this modification the design proposed here presents some advantage in terms of gate usage and spectral dynamic range.*

# 1 Introduction

In the hybrid correlator proposed for ALMA, a large fraction of the total logic and correlator cost is represented by the digital filter bank. Since the circuit is replicated in a large number of copies, even a modest reduction in complexity may have a relatively large impact on overall system cost.

In report [8] a two stage tunable filter has been presented. The design, shown in fig. 2, is composed by a complex oscillator and mixer, a first decimating "broad" filter, a second "sharp" filter, and a complex to real conversion stage. The first filter has a road transition region, and thus a short FIR response time (128 taps). The second filter operates at the decimated frequency, allowing for a long response, and a sharp transition region, with only 64 taps. Both filters have complex samples and real coefficients.

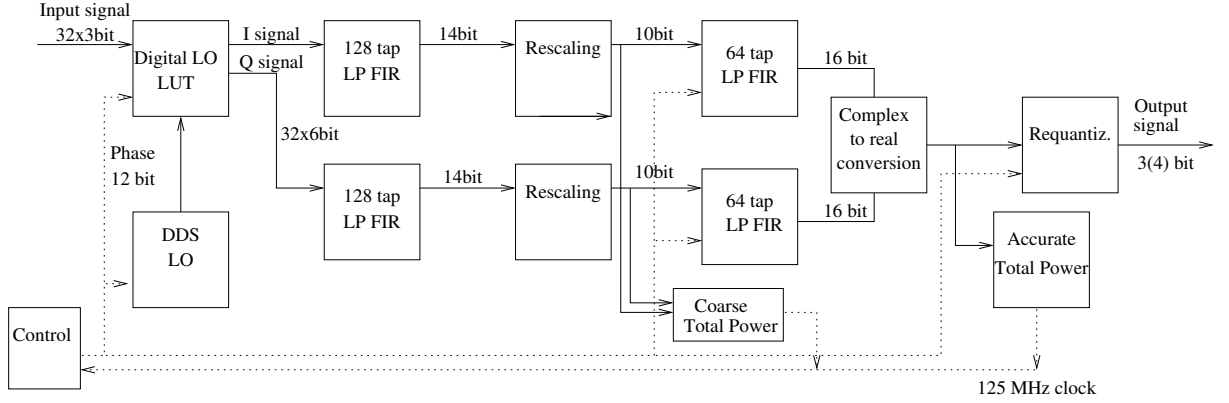


Figure 1: Structure of the original digital BBC. The signal is downconverted by a digital LO/mixer, filtered by a first broad filter, re-quantized to 10 bit, filtered by a second sharp filter, converted to real representation, rescaled and re-quantized to a final resolution of 3 or 4 bits. Total power meters are used to monitor signal level.

A modified architecture (fig. 2), with almost identical performance and response, may be obtained moving the LO/mixer after the first filter. The first filter has a bandpass corresponding to the desired portion of the input spectrum (without restrictions due to decimation), and is obtained from a the low pass prototype used in the previous approach, translated by a frequency equal to the LO setting.

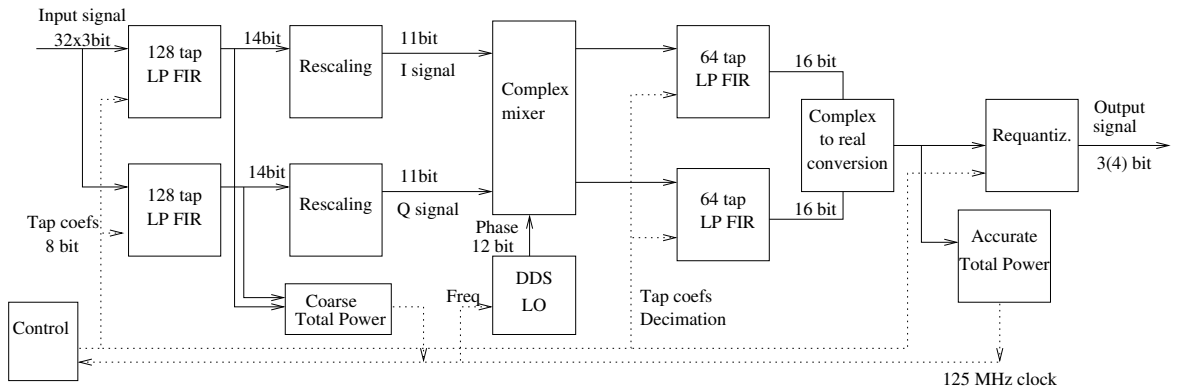


Figure 2: Structure of the modified digital BBC. The signal is first filtered by the broad filter, decimated, and then frequency converted by a full complex mixer. The second filter and output section is identical to the previous case

The filter is thus depending on the sub band position, and its coefficients must be reloaded every time the tuning change. To avoid aliasing, it must discriminate between positive and negative frequencies, It has therefore

real input, complex (hermitian) tap coefficients, and complex output. The mixer/LO is fully complex, with 4 multipliers and 2 adders. The second filter and complex-to-real conversion stage is identical to the previous design.

The main advantage of this design is that the mixer operates at the decimated frequency. Since a time multiplexed mixer is composed of 32 identical multipliers, even considering for the increased complexity in the multi-bit complex multiplier this results in a drastic simplification. It is possible to use a much better multiplier, thus increasing the global quantization efficiency (although by a small value, about 0.5%) and spurious free dynamic range.

Another advantage is that the first filter operates on the 3-bit input data representation, instead of the 6-bit mixer output. This reduces the total filter size by a considerable amount (30-40%).

A further advantage is that the mixer does not see any DC component that can be produced by an offset in the sampler thresholds, as this is effectively filtered by the first filter. This DC component is equivalent to a strong monochromatic line, and may produce undesired spurs as it beats with the LO harmonics.

## 2 Theory of operation

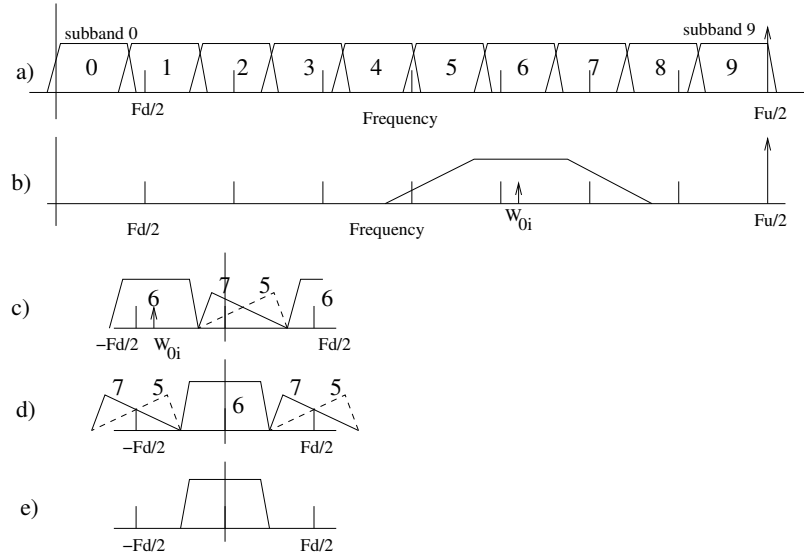


Figure 3: Spectral processing example. For readability, a x8 multiplexing factor has been assumed, instead of x32. From top: (a) Input real signal, divided into 10 sub bands; (b) Undecimated and (c) decimated broad filter output; (d) Mixer output; (e) Sharp filter output

Signal processing for an hypothetical 1:8 decimated signal is shown in fig. 3. The real input, divided in 10 overlapped sub-bands, is shown in (a). The broad filter selects sub-band 6, with guard bands from sub-bands 5 and 7 (b). After decimation, (c) the band of interest occupies half the complex decimated bandwidth, with sub-bands 5 and 7 aliased in the remaining half. In the particular case, the band of interest folds from positive back to negative frequencies. After complex mixing the band of interest is centered on frequency zero (d), and the unwanted sub-bands are rejected by the sharp filter (e)

The processing of a real simulated signal, with the desired 1:32 decimation factor, is shown in fig. 4 and 5.

The signal is the same used in the previous report. The complex spectrum of the (real) input signal is shown in fig. 4a. The signal is composed of white noise, a strong out-of-band tone (-20dB), and a weaker (-30dB) in-band tone. The simulated signal is 2.5 ms long.

After filtering, the signal is shown in fig. 4b. Only one side of the complex spectrum is preserved, thus avoiding undesired aliasing in the decimation operation.

After decimation, the signal has the spectrum shown in fig. 4c. Even if the spectrum folds from positive to negative frequencies, no undesired alias of the strong input line can be seen.

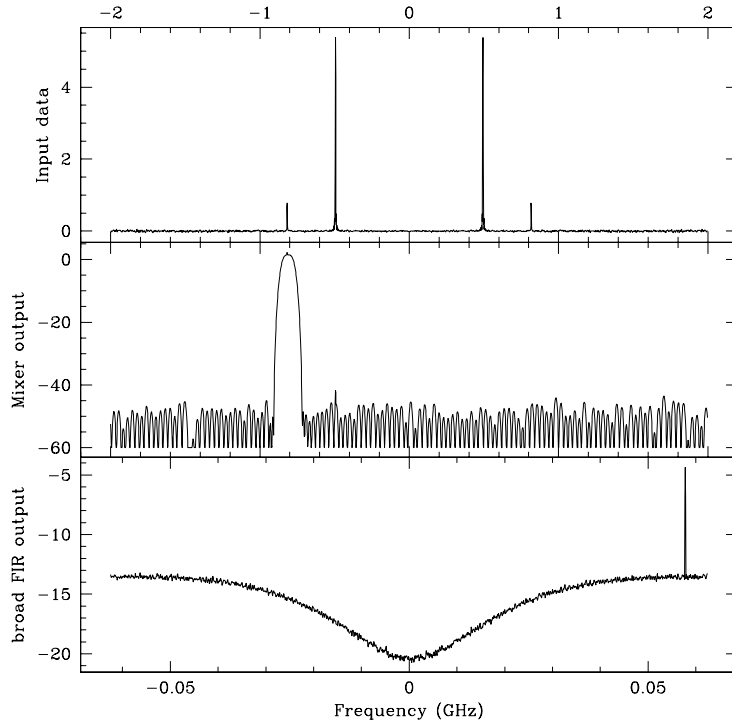


Figure 4: Spectral processing of a simulated signal. From top: (a) Input real signal; (b) Undecimated and (c) decimated broad filter output. Graphs have a logarithmic (dB) scale.

The complex mixer rotates the filtered spectrum in order to present the desired passband to the sharp filter centered on frequency zero (fig. 5a). The low pass sharp filter then selects the desired passband and removes the undesired passbands (5b). This signal is then converted to real (5c), and re-quantized for correlation. The filter real output is exactly equal to that of the filter described in the previous report (apart from quantization effects).

## 2.1 Broad band filter

The filter is a complex passband (real samples, complex coefficients) derived by the low pass prototype used in the previous design. The prototype has a bandpass equal to  $1/64$  the input bandwidth, and a guard region twice as large. After decimation, both the complex response and the two guard bands have a total width of  $1/32$  the initial band, or  $1/2$  the decimated complex band. The two guard bands fold in the same region of the decimated band.

The prototype is shifted by the desired center frequency. For 34 sub bands, the rotation for channel  $i$ , ( $i = 0, 33$ ) is  $(i - 0.5)/34 \times 2$  GHz, but arbitrary shift is possible. Thus, filter tuning is accomplished by calculation of a new set of coefficients (no filter optimization is necessary) and reloading of the coefficient memory.

The real part of the filter is symmetric, while the complex one is antisymmetric. In both cases, filter structure may exploit this symmetry to reduce the number of multiplications. Filter conceptual schematic for the real (symmetric) branch is shown in fig 6. The demultiplexed inputs are fed to 32 identical groups of four taps each. Direct and inverse taps are summed together before multiplication.

Folding and summing corresponding samples may present problems in a few-bit representation. The input samples are not actual values, but arbitrary codes. Summing the codes obviously does not work. The code is neither monotonic, nor equispaced. The signal must therefore be converted to a monotonic, equispaced code before the filter. This imposes a limitation on the possible quantization codes, resulting in a slightly reduction in quantization efficiency. A equispaced code (values 1, 3, 5, 7) has an quantization loss of 3.??%, against a loss

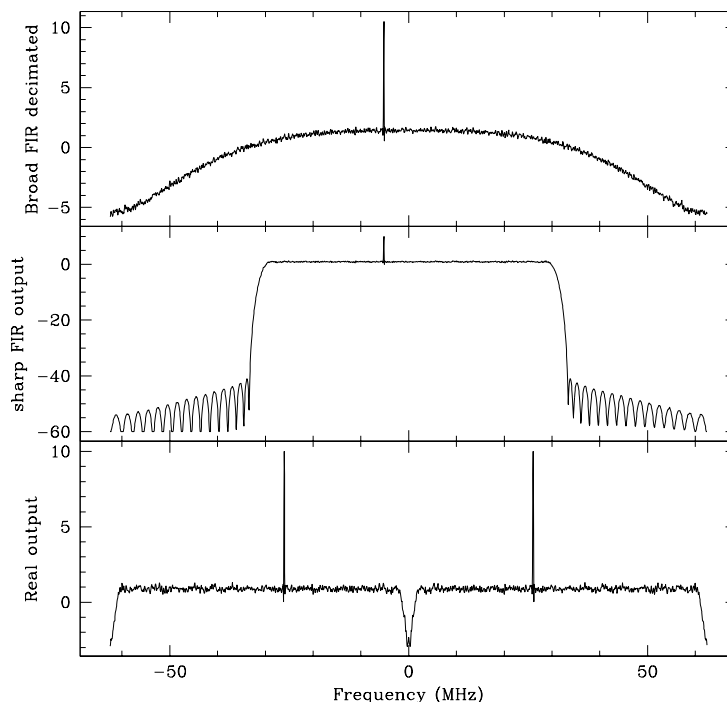


Figure 5: Spectral processing of a simulated signal. From top: (a) mixer output; (b) Sharp filter output; (c) Real signal sent to the correlator. All plots are on a logarithmic vertical scale.

of 3.??% of the more efficient code 1, 3, 5, 8, and a theoretical minimum loss of 3.??%.

The result of the sum of two codes (1, 3, 5, 7) can be any even number from  $-14$  to  $14$ , representable with a 4 bit, signed quantity. For 8 bit signed coefficients, product size is 11 bit. Filter multipliers are therefore implemented with 16x11 bit RAM blocks.

The filter has been designed using the filter from the previous design as a low-pass template, and multiplying each coefficient by the appropriate exponential.

The same considerations about coefficient precision truncation apply for here. The actual filter shape, however, depends very much on the local oscillator setting. Truncation is an intrinsically nonlinear procedure, and only statistical properties of the filter shape can be anticipated.

An alternative approach would be to use a nonlinear minimization program to adjust filter coefficients on the desired shape after filter rotation, instead of blindly truncate them. This approach would probably give a better stop band rejection (by 2-3 dB), at the expense of a much higher computational effort during filter reprogramming.

## 2.2 Complex Local Oscillator

The local oscillator is greatly simplified with respect to the previous approach. It is composed by a DDS register, similar to the previous one, that generates a 10 bit phase value. No phase offset is needed, apart from the 90/180 degree phase switching. The 10 bit value is fed to a sine/cosine lookup table, that produces a high resolution sine and cosine value. A complex multiplier, implemented with four hardwired multipliers and two adders, compute the expression  $y(t) = x(t) \exp(2\pi j\nu_0 t)$ .

The mixer does not select the bandwidth, it must only compensate for the unwanted rotation of the filtered band, and for its possible folding from positive to negative frequencies (as in the example shown in fig. 4). The complex mixing rotates the decimated band in order to have the frequency scale monotonically ordered from  $-62.5$  MHz to  $+62.5$  MHz. After conversion, the desired band is centered around frequency zero, and therefore

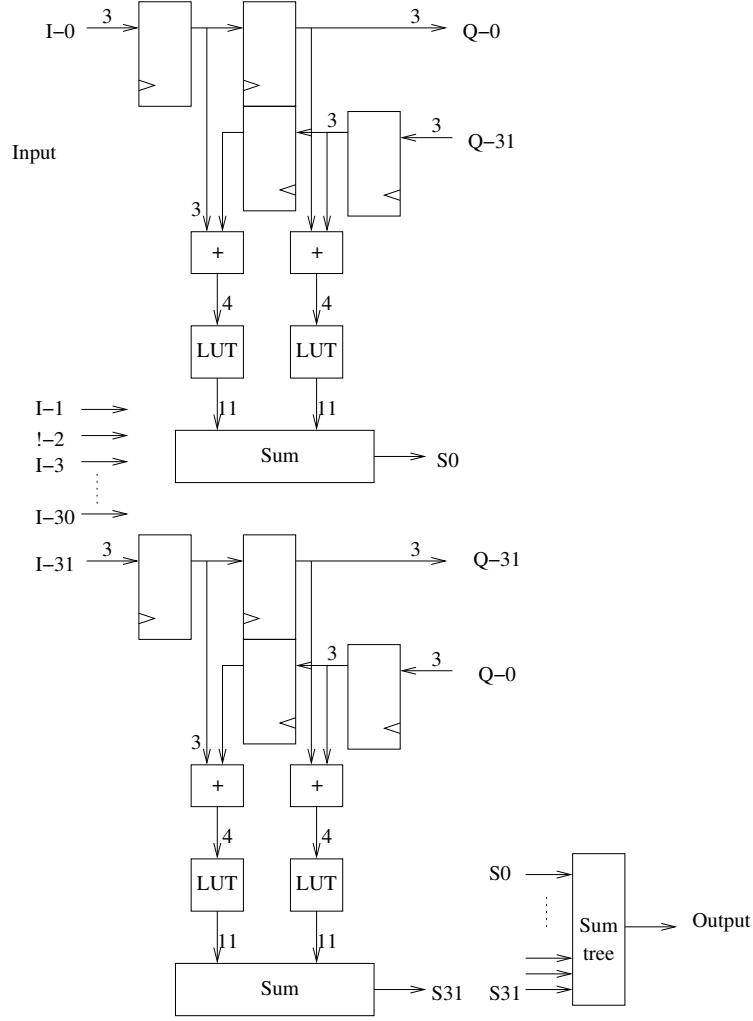


Figure 6: Coarse FIR schematic. Signals from I and Q mixers are multiplied by coefficient taps in LUT tables. Input is from 32 time multiplexed streams, output is to 2 (I and Q) streams.

can be filtered by a low-pass filter.

The local oscillator value is programmed to the desired LO frequency  $\nu_0$  modulus 125 MHz. The remaining part of the LO frequency affects only first filter coefficients, as bandwidth selection is done in this filter.

The phase quantization step affects LO harmonics content. With 1024 phase bins, the first harmonic appears at harmonic number 1024, with an amplitude of approximately -60 dB. Amplitude quantization in the sine/cosine table also generates harmonics, but with 8 bit sine/cosine representation the spur free dynamic range is around -70 dB.

To reduce harmonic content, a small (few phase bins) pseudo-random noise can be added to the DDS phase. The resulting phase jitter is of the order of 1 degree, but is multiplied by the harmonic number, completely washing out the harmonics due to phase quantization.

The lookup table can be simplified if only first quadrant values are stored, and the sign is treated separately. In this way, lookup table size is reduced to 1/4, and one more bit is available for the result.

### 2.3 Sharp filter and output section

This section is identical to the design described in [8].

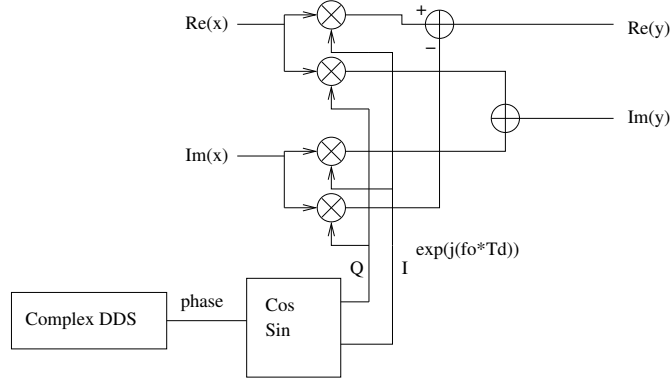


Figure 7: Complex local oscillator. A DDS register generates a phase value. Sine and cosine values are generated in a lookup table. The complex multiplication is implemented in 4 hardwired multipliers and two adders

### 3 Considerations on FPGA resource usage

Implementation of this filter require considerably less resources than the previous design.

The broad filter has 3 bit input, instead of 6. This requires about half the resources in terms of configurable blocks, lookup tables. The saving in the adder chain is not so high, since most of the adder tree size is dictated by the coefficients size, not by the samples size. The lookup tables must be writable. This increases its complexity, especially in terms of routing resources.

The mixer multiplier must be implemented using hard multipliers, not lookup tables. A single large lookup table to hold sine/cosine values is still needed. Especially for Altera FPGAs, this is a large advantage, as these chips have smaller RAM blocks, but also one or two large RAMs.

Re-tuning the band is relatively slower, the filter has no capability for frequency hopping. This is not a requirement, and tap reloading is in any case faster than for a full 1024 tap filter. Some intelligence is needed in the control processor to recalculate filter taps from the low-pass prototype, but this is within the capabilities of any current microprocessor.

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