Atacama Large Millimiter Array
A MMIC sampler for ALMA - Design report

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Abstract

A sampler circuit for the Atacama Large Millimeter Array, based on a GaAs 0.12 μm process, has been designed and tested by simulation. The use of a separate sampler before the BiCMOS digitizer allows a longer time for quantization decision, and reduces the timing requirements on the digitizer. The predicted performances fulfill the requirements for the ALMA sampler/digitizer. In particular the aperture time is < 50 ps, and the bandwidth in excess of 4 GHz. The chip is now being fabricated and will be tested in spring 2002.

1INTRODUCTION

The Atacama Large Millimeter Array [9] is a joint project of the USA, European and Japanese radioastronomical communities for a radio interferometer. It is composed by 64 to 96 radio telescopes of 12 m diameter, operating from 31 to 950 GHz. It will be sited in the Atacama Altiplano in northern Chile, at an altitude of 5000 m, north of the VLT site, and is planned to become operative starting from 2005, with full capability in 2010.

Each antenna observes a maximum bandwidth of 8 GHz, implemented as four 2 GHz sub-bands, simultaneously in two polarizations. Thus, a total of 8 independent radio signals (IF's), with a bandwidth of 2 GHz each, is generated by each antenna.

The output of each IF is represented by a signal at nominally 13 dBm (1V RMS), with a bandwidth comprised between 2 and 4 GHz. It must be sampled and quantized to a stream of 3-bit digital samples (8 levels), at a rate of 4 MS/s.

Most existing radio telescopes use a digitize-first approach for signal sampling and digitization. In this approach the analog signal is first compared to a set of thresholds, obtaining a stream of digital signals. These signals are then sampled using an array of digital latches clocked at the appropriate frequency. This approach has the advantage of a great simplicity, since the digital latch operates only on logic levels. Moreover, a digital latch is needed in any case and no separate sampler unit is required.

The other possible approach, commonly used in multi-bit digitizers, consists in first sampling the signal, using a sample/hold circuit, and then digitizing the stable samples so obtained. This approach (sample first) is useful to overcome non idealities of the comparators, especially in their dynamic performances (e.g. skew in propagation delay, or its dependency on signal amplitude). A Sample/Hold or a combination of Sample / Hold or Track/Hold[1] before the digitizer allows one full sample period (typically half the clock period) for setting and decision, and this regardless of the sampled voltage.

In this report we describe a Sample/Hold chip to be used in a sample-first approach for the ALMA digitizer. Digitizer requirements are described in chapter 2. Different possible approaches for the sampler are considered in chapter 3. The proposed circuit is described in chapter 4, with individual blocks analyzed in

[1] A Sample/Hold is characterized by a hold time much longer than the sampler time. In this report we propose a Track/Hold circuit (hold time approx. equal to half the clock period), but will use the term *Sampler* or *Sample/Hold* for simplicity.

chapter 5. The circuit has been simulated, with simulation results presented in chapter 6. Future plans for this work are discussed in chapter 7.

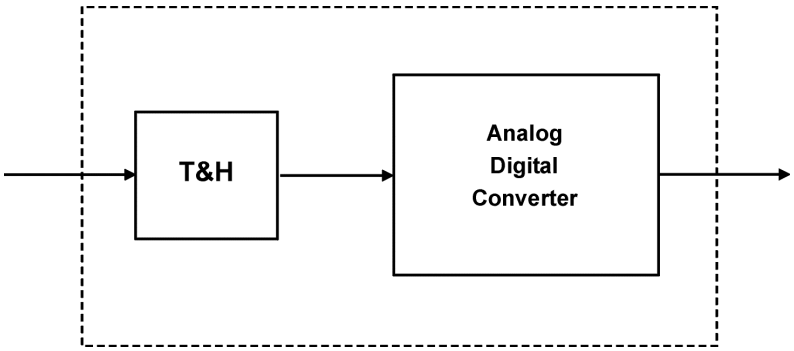


Fig. 1: Sampler/digitizer unit

2REQUIREMENTS OF THE SAMPLING CIRCUIT FOR THE ALMA DIGITISER

2.1ALMA PROJECT SYSTEM REQUIREMENTS:

The ALMA digitizer specifications [10] are rather tight, and a rapid survey of commercial or existing scientific units has not found a directly available unit. Some of these specifications are from a private memo by Larry d'Addario, and although they have not been incorporated in the final specifications and are thus to be considered tentative requirements, they have been considered in the chip design.

- **Inputs**:
  - **Analog signal**: 2 to 4 GHz nominally 0dBm (0.23 V rms)[2], with zero-mean gaussian probability distribution. Input signal must be correctly digitized when the input signal is in the range -2σ to $+2\sigma$, with σ the RMS input level. No damage shall occur for –1.5 to +1.5 V. Nominal input impedance is 50 Ohm resistive. The input pin shall have an adjacent analog ground pin; the VSWR across these pins shall be <2.0 over 2.0 to 4.0 GHz. When driven from a 50 ohm source, the frequency response of the on-chip analog circuitry shall be flat within +/-0.5 dB over 2.0 to 4.0 GHz.
  - **Sampling clock:** 4 GHz, nominally sinusoidal, 0.5v p-p, any convenient D.C. level**.**
- **Output:**
  - **Digitized sample:** 3 bits as 1s complement, 4Gb/s each. Sample clock 4 GHz. parallelized output at 1/32 the input clock
  - **Delayed version of sample clock input**: timed to accompany digitized sample outputs**.**
- **Timing:**
  - **Sampling aperture time:** 50 ps with a sampling stability, relative to external sampling clock, of 1 ps max rms. jitter in 10 s averaging time. Optionally sample clock phase may vary to implement fine delay control.

[2] Old specifications indicate an input signal level of 0 V RMS (13 dBm). Chip has been designed with capability for high level signal. Successive versions will be optimized for a signal level of 0 dBm.

- **Linearity and accuracy:**
  - **Quantising thresholds:** derived via a resistor ladder from two external voltages, continuously adjusted to match the input signal mean and RMS values. The extreme thresholds are at about +/- 1.6σ
  - **Linearity:** better than 2% in the range between the extreme thresholds (nominally +/- 1.6 σ)

2.2MOTIVATIONS FOR A SEPARATE SAMPLER/HOLD UNIT

To implement these specifications, a SiGe digitizer has been designed by the Electronics Engineering department of the University of Bordeaux[11]. It is based on the quantized-first approach, and in principle can be operated as a standalone unit. In parallel, a sample/hold circuit has been designed at the Arcetri Observatory and the University of Florence of MECSA. This unit can be used in front of the Bordeaux sampler to implement a sample-first design. This would relaxes several specifications on the digitizer unit, with a moderate increase in total system cost.

2.3SPECIFICATION FOR THE SAMPLER UNIT

These specifications reflect to various aspects of the sample/hold circuitry. The input bandwidth extends to the sampling frequency, while usually samplers are characterized up to half the sampling clock. High bandwidth coupled to high flatness imposes a very narrow aperture window, better than 50 ps (corresponding to an attenuation of -0.58dB at 4 GHz). The high input level, together with the stochastic nature of the signal, gives rise to very high slew rates, that must be followed by the analog circuitry. The possibility of high spikes in the signal (up to 5-6 V) imposes some form of signal clipping at the input.

Both the feasibility study and circuit design for the sample/hold circuit have been based on a subset of the above specifications, listed in the following table. In particular several different system architectures and circuit topologies have been taken into account in order to match the objectives highlighted in the previous paragraph.

SPECIFICATION	
Input Signal Bandwidth:	2 GHz (2 - 4 GHz)
Sampling Frequency :	4 GHz
Number of Equivalent bit :	5.5 bit (2% accuracy)
Clock Signal:	0.5 Vpp (Nominally Sinusoidal)
System Impedance:	50 Ohm
Nominal Input signal level	0 dBm (230 mV RMS) Gaussian noise
Acceptable Input Signal Level	+/- 10 V, clipped at +/- 1.8V

3FEASIBILITY STUDY

3.1INTRODUCTION

Different topologies and configurations have been evaluated in order to develop the sampling subsystem for Alma digitizer. The choice has been done on the base of the different requirements for the sampling subsystem and comparing the advantages and drawbacks of the different configurations.

The block diagram of a generic sampling circuit is shown in fig. 2. The most critical block is the Switch, that determines the dynamic performance (aperture window) and the accuracy of the sampled signal (insulation in the off state, tracking speed)

In particular three different topology for an electronically controlled switch based on FET or Diode Switch have been evaluated.

The most important error that may affect the sampling circuit are related to the switch behavior.

These error are:

1. *Aperture time:* It is due both to finite rise time in the generated clock signal, and finite response time in the switch. Produces attenuation at the higher input frequencies and non ideal frequency response
2. *Feedthrough:* It is due to cross-talk between the switch input and output due to parasitic capacitance in the hold state
3. *Jitter error:* non deterministic phase error in the clock signal. It seriously degrades the phase response of the sample

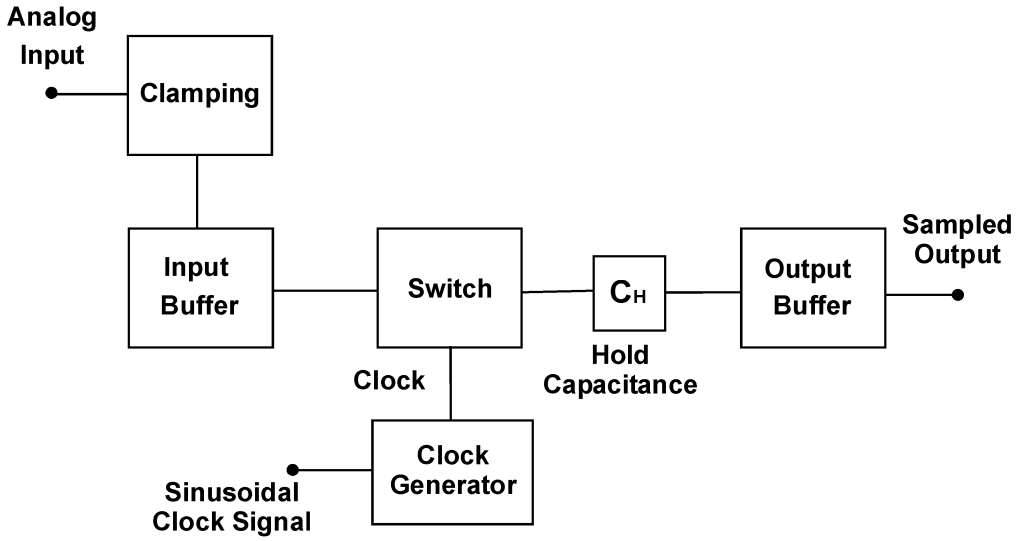


Fig. 2: Generic block circuit for a sampler

Balancing between good performances with respect of these error, and matching with target requirements has been at the base of the choice for the configuration.

The switch may be implemented following two different approach:

1. FET switch :

   Better behavior with respect of *feed through* (less parasitic capacitance)

   Better accuracy

2. Diode Bridge Switch:

   Best behavior with respect of *input signal dynamic*

   Less distortion at high frequency

3.2 DIFFERENTIAL FET SWITCH

A differential FET switch configuration, shown in fig. 3, consists of an input stage that operates as a switched source follower sampler, a switch driver and an output buffer. It presents several advantages for a circuit with a high sampling rate. In particular the intrinsic features of this configuration include: high linearity, small pedestal error, large input voltage range and an high sampling rate. It consists of an input stage that operates as a switched source follower sampler, the switch driver and the output buffer.

A fully differential implementation of this configuration is highly recommended in order to improve overall linearity, common mode pedestal noise and to reduce the effective drop rate.[4]

The main drawback of the fully differential approach is in the high number of circuit elements that have to be used to implement the S/H. Another problem is that simulations have shown that this circuit cannot correctly maintain the interdiction state for large amplitude input signals, since the transistors are driven outside their correct polarization regime.

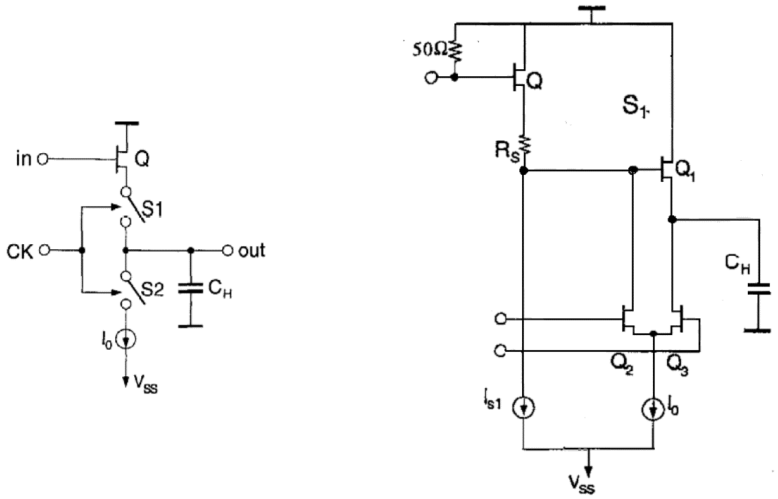


Fig. 3 - Differential Switch FET (one half of fully differential design)

3.3SELF INVERTING FET SWITCH:

This configuration is based on a quite simple but highly efficient FET switch based on a shunt series architecture, as shown in fig. 4.

This topology is compatible with large input signal dynamic and with high sampling rate. It requires a control clock signal with a voltage swing of 1 volt, simplifying the generation of rise and fall fronts having timing compatible with the project requirements.

Another important feature of this topology is the high compactness, allowing a simple implementation of a single chip S/H circuit. [2]

For all these advantages with respect to the other configurations, we have chosen this topology for our sampler.

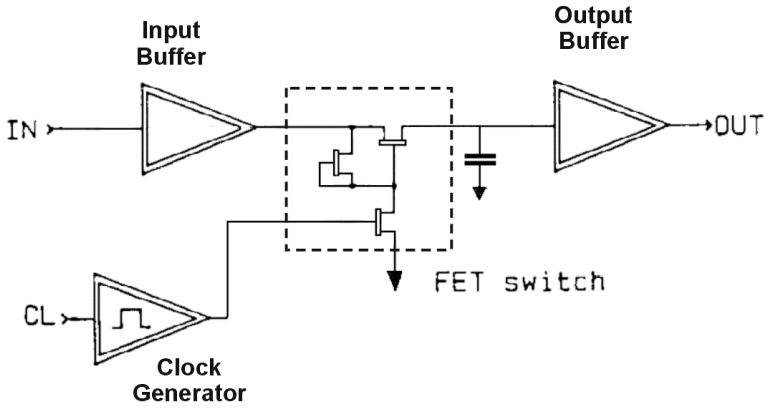


Fig. 4 - Self Inverting FET Switch

3.4DIODE BRIDGE SWITCH:

A diode bridge (fig. 5) offers in principle a larger input signal range and less high-frequency distortion at the expense of greater feed through and less accuracy. The input is directly coupled into a sampling bridge consisting of six diodes. The purpose of the two diodes in the center the bridge is to provide a low impedance return path for the clock current in the Hold state, to prevent unbalanced behavior of the ECL driver circuit.

The diode bridge is used as a switch. An ECL clock signal (single or differential) enters the clock driver [1] which control the bridge. When the clock is high the diodes are driven in a conducting stare, and the bridge is in the sample mode. When the clock goes low, the bridge is in hold mode, insulating the input from the hold capacitor and the output driver.

In this particular application, due to the very large dynamic of the input signal (a white Gaussian noise 1V rms.) this configuration would require a very high level for the ECL clock control signals, in order to correctly polarize the diodes. Test on this configuration have point out that these high levels, together with the increased diode capacity and depletion times, are incompatible with a rise and fall time of the ECL control clock of about 50 ps as required. Therefore this configuration has been rejected.

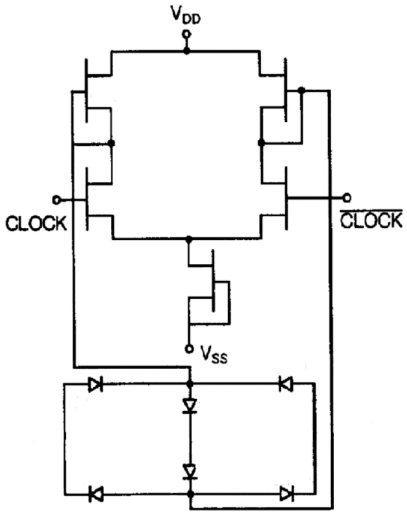


Fig.5 - Diode bridge Switch

4BLOCK DESIGN FOR THE SAMPLER CIRCUIT

4.1INTRODUCTION

The Sample and Hold has been developed following the idea of a single chip system. All the functional blocks have been implemented on the same chip, including the level shifting circuits for the generation of the biasing dc levels, and all the choke capacitance need to ensure the absence of spurious signal on bias voltage. Only external voltages of +3V, -3V and -6V are required.

This approach allows an optimum control on the performances of the system (being all the component on the same chip all the devices show the same performances) and less space occupation. In particular, due to the fact that most of circuit depend upon the ratio among the dimension of the devices used in the circuit, the system on a chip approach allow a good control on the performances.

Circuit protection against wide dynamic signals (clamping circuit) and wide band matching (50 Ohm system impedance) is present at the input circuit.

The chip has been implemented using the Philips ED02AH P-HEMT process. This technology is available for prototyping and small volume production (hundreds to thousands of chips, adequate for ALMA requirements) through Circuits Multi Project (Grenoble).

The main features of ED02AH technology are summarized below [3]:

1. Hetero-epitaxy with a pseudomorphic (GaInAs) active layer
2. Depletion and enhancement mode recessed transistors: Vt=0.1V or -0.9V
3. 2 types of diodes (0.2µm "GM" and 3µm "BE") for mixing, level shifting, or varactors.
4. Resistors, using the GaAs active layer, non etched.
5. Full Si_3N_4 protection ensuring high reliability
6. 2 types of MIM capacitors, using the Si_3N_4 layer and the Si_3N_4 + SiO_2 layer.
7. SiO_2/Si_3N_4 + air bridge isolation between layers to reduce the parasitic capacitances.
8. High yield 1.25µm thick gold metallization for interconnections and spiral inductors. Possibility of multi metal lines to reduce series resistances.
9. Via holes through the 100µm substrate to reduce parasitic inductances to ground.

4.2 SCHEMATIC BLOCK DIAGRAM

The sampler is organized on the base of a certain number of functional blocks, shown in fig. 2.

A clamping circuit (based on diodes) guarantees the protection against high level input signals, effectively shorting to ground signals greater than about 1.8V.

The input buffer ensures high input impedance and provides the low impedance required to drive the sampler switch. It also insulates the input signal from the switch.

The switch implements the sampling function, together with the hold capacitance. It is driven by a square wave clock signal, provided by the clock generator.

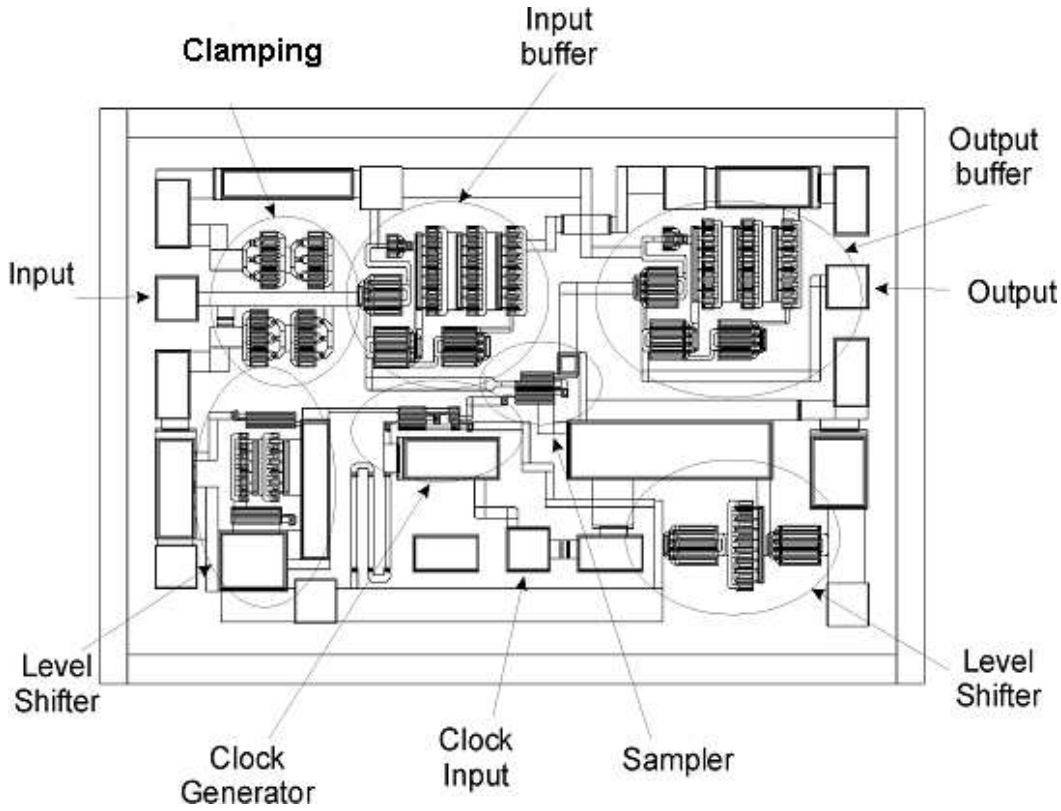


Fig.6 - Sampler layout

The output buffer supplies the high input impedance that must be seen by the hold capacitance, and the required 50 ohm output impedance.

The chip contains also two level shifter for the on chip generation of bias voltage levels starting from that supplied from the system (+3V, -3V, -6V).

4.3LAYOUT

Circuit layout is shown in fig. 6, with functional blocks highlighted. Chip dimensions are 1.5x1 mm. Input, clock and output pads are configured for 3-finger radiofrequency probes, with finger spacing from 150 to 200 ?m. The production chip will have only bonding pads, thus reducing chip size.

A second chip with separate individual blocks has been designed, to allow separate characterization of these blocks.

Individual blocks are described in more detail in the next chapter.

5FUNCTIONAL BLOCKS

5.1SAMPLING CIRCUIT

The sampling circuit has been implemented using a FET Self Inverting Switch architecture, that is a configuration based on a shunt series topology. Its schematic is shown in fig. 7.

One of the most important feature of this topology is the self inversion of the clock signal supplied by the shunt branch, that enable the use a single clock signal to drive both shunt and series switch.

This approach allows a great simplification in the clock generation circuit, avoiding the problem related with a two-phase square wave, as required in the diode bridge and differential FET switch. [4], [5],[6]

Furthermore the applied bias voltage and the signal dynamic allows the switch to be correctly driven by a square wave clock signal with a 1V amplitude, that enables the use of simple clock signal generator compatible with the system requirements (50 ps rise time)

Moreover this topology is compliant with the large dynamic of the input signal, that causes great problems both for the diode bridge topology and for the fully differential FET switch. [2]

The bias voltage (-4V) has been chosen with respect of the input signal dynamic after the clamping circuit (+2 V: -2V). In particular this bias voltage ensure the two shunt inverting FETs work always in the saturation region and quite far from the breakdown or the linear regions.

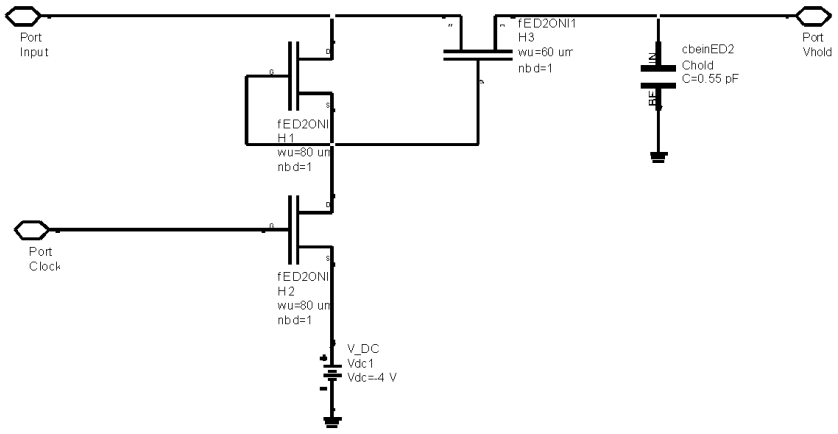


Fig. 7 - Sampler Circuit

5.2CLOCK GENERATOR

This block generates the square wave clock signal from the 0.5 Vpp clock sinusoidal signal supplied from the system. Its schematic is shown in fig. 8. It contains also the level shifter used to supply the bias voltage not externally provided (-3.5 V).

The circuit is composed by a common source stage followed by a common drain. [7] The first stage generates the quasi square wave signal while the other behaves as a buffer offering the first stage an high input impedance. The buffer stage provides a signal with the low output impedance needed to drive the sample and hold circuit

The circuit is AC coupled to the input signal. The DC block capacitance and the two stages also shift the sinusoidal clock signal to the desired DC level of about -6 V.

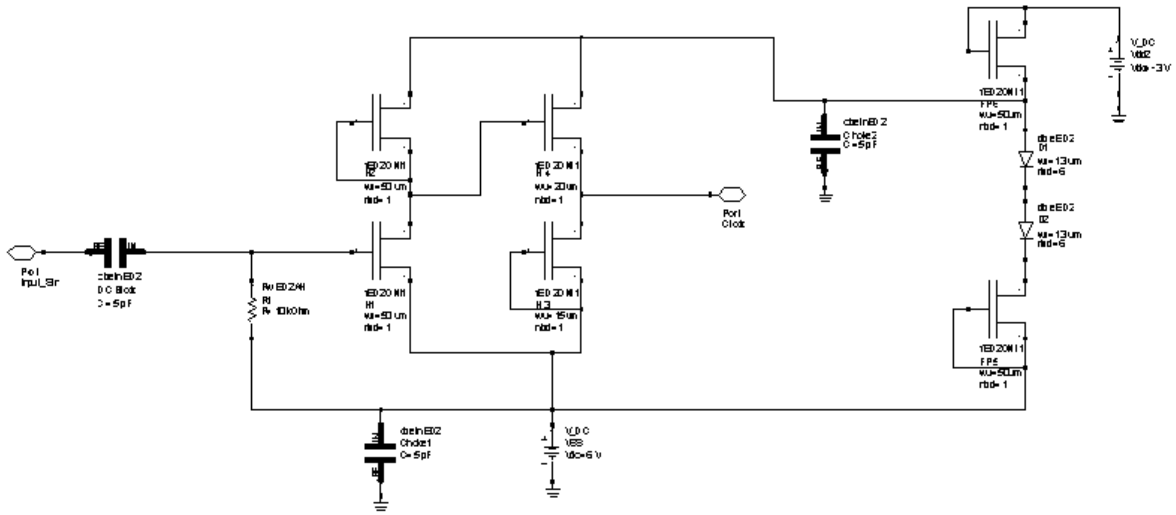


Fig.8 - Schematic of Clock Generator circuit

In fig. 9 the square wave generated by the circuit is shown, superimposed to the ideal square wave. The comparisons between the ideal and real clock signal highlight a good agreement with the specification and in particular a rise time of about 50 ps.

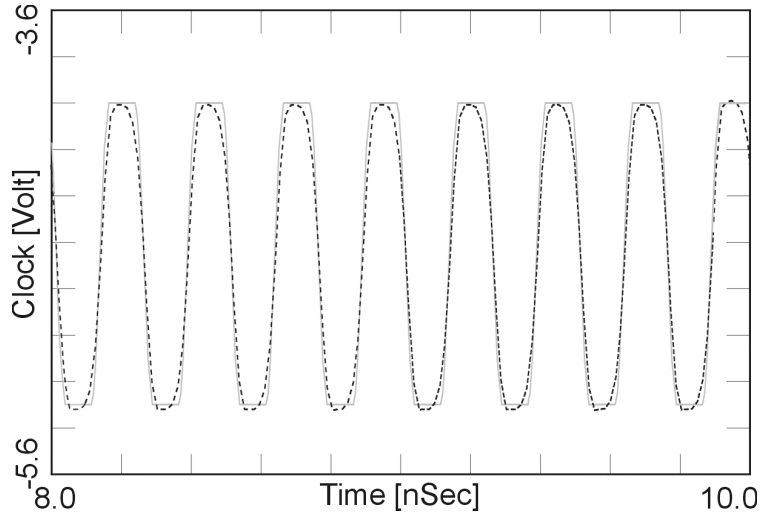


Fig. 9 - Square wave generated by clock generator

5.3 INPUT AND OUTPUT BUFFER

This block has been used to implement both the input and output buffer. The first buffer supplies a high input impedance, to simplify input matching, and drives the sampler circuit with a low value of output impedance. The second one shows a high impedance to the hold capacitance in order to prevent a quick discharge in the hold phase, and drives the low impedance output of the circuit.

This buffer, which schematic is shown in fig. 10, is a complex version of the source follower configuration, optimized to maximize the input and minimize the output impedances. The circuit is also designed to minimize the insertion loss and maximize the bandwidth. This aspect is very important for the output buffer whose band has to be much larger than the input signal bandwidth due to the presence of the high order harmonics generated by the sampling process.

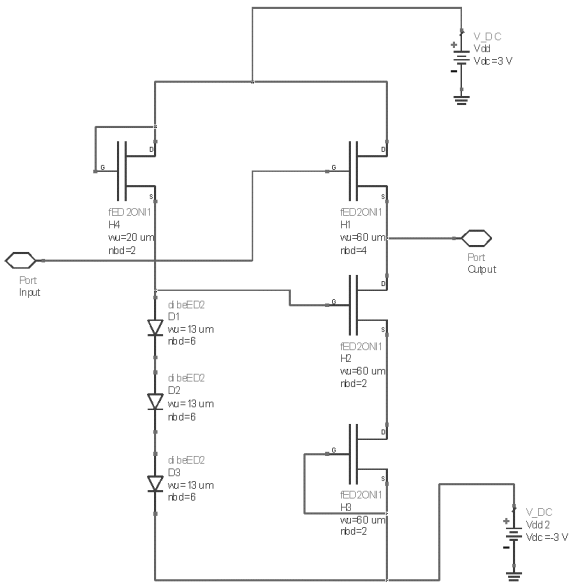


Fig. 10 - Input and output buffer circuit.

Particular care has been taken in the dimensioning of the components in order to minimise the DC power consumption. As a matter of fact, HEMT and diode dimensions have been chosen on the base of a trade between different and conflicting requirements.

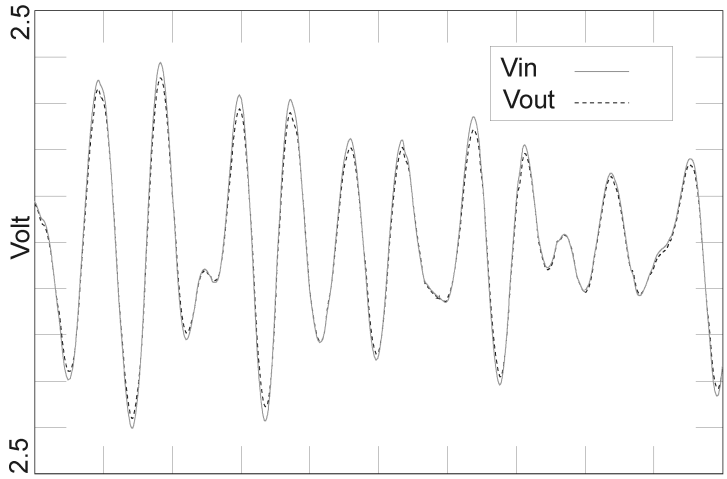


Fig. 11 - Input and output buffer response to the white gaussian noise

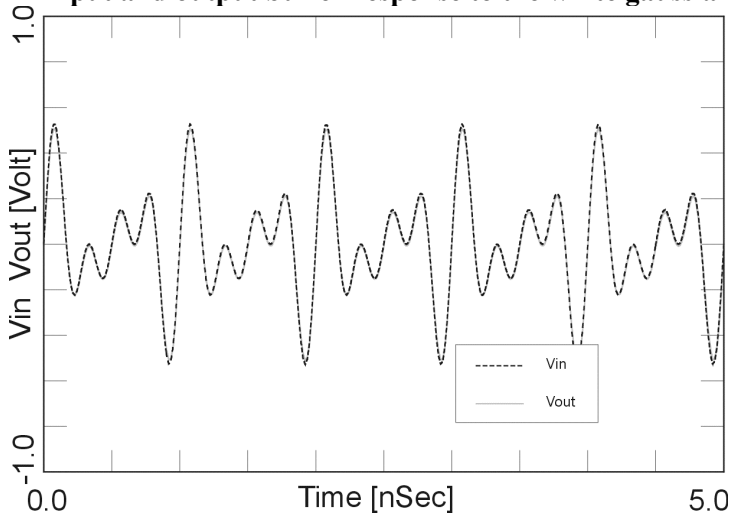


Fig. 12 - Input and output buffer response to a composite signal

6SIMULATION TESTS ON THE CIRCUIT

The circuit performances has been evaluated simulating the response with respect of the different input signal. All tests have been performed using the Agilent HP-MDS 7.01 Microwave cad simulator, together with the device models provided by the manufacturer (ED02AH library version 2.1 from OMMIC through CMP) [8] for this process. Precedent experience has shown that these models predict in a very reliable way the actual behavior of circuits manufactured using this technology.

In particular three different input signal have been used:

1.3 GHz Sinusoidal input.

2.3.95 GHz Ideal Square Wave input

3.White Gaussian Noise Signal

The sinusoidal input has been used to evaluate the performance of the system in the center of the input bandwidth.

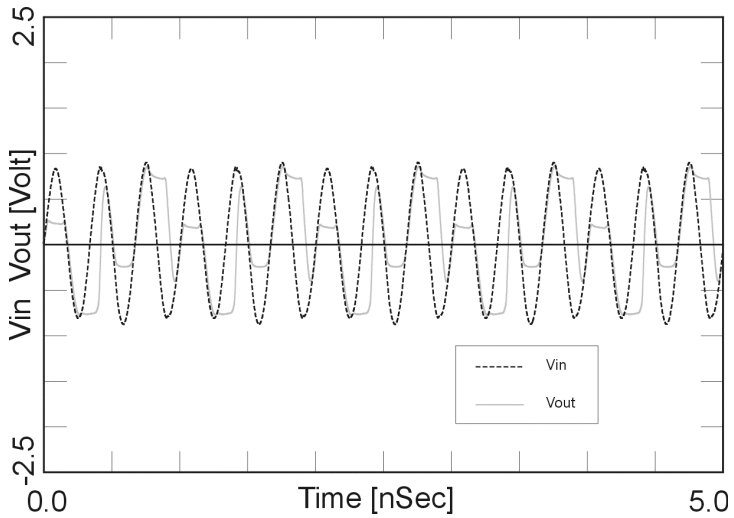


Fig.13- Sampler output @ 3GHz sinusoidal input

The square wave signal has allowed the evaluation of the aperture time of the system that is a critical feature for the circuit. Due to high input bandwidth (up to the sampling frequency of 4 GHz) an aperture time sorter than 50 ps is necessary to ensure a flat bandwidth. Using an ideal square wave at a frequency close to the sampling frequency, the sampler output is represented by the integral of the sampling function, that can be accurately measured.

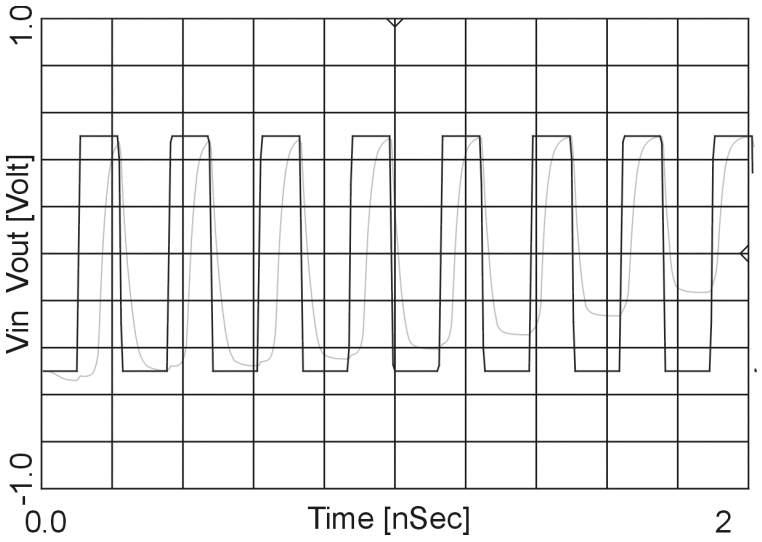


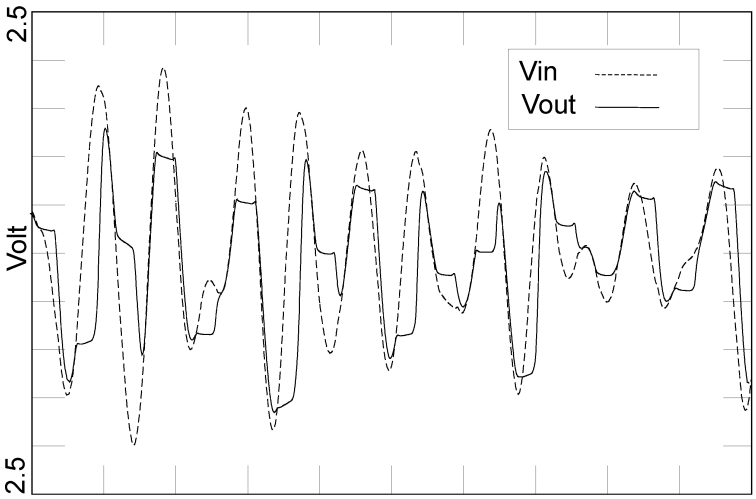
Fig.14 - Sampler output for a 3.95 GHz square wave input

The white Gaussian noise input with 1 Volt RMS has been used to evaluate the performance of the sampler to an input signal close to the real one. Since a 1 V RMS signal may have transients with an amplitude of several volts, the performance of the input clipping circuit is also evaluated by this test, together with the behavior of the circuit at extreme voltages. Clipping has been shown to occur at about 1.8V, and the signal at the input buffer never exceeds an amplitude of 2V.

Fig.15 - Sampler output for a White Gaussian Noise input

All the three test has showed positive response and the performance of the sampler matches the requirements of the system. Some critical parameters have been measured.

- Aperture time is better than 50 ps. It depends somewhat on the input signal level, being larger for large signals.



- Insulation in the hold state is 38 dB. Some feedthrough is visible, especially with the large swing Gaussian signals. A compromise between insulation and aperture time has been found optimizing switch FET dimensions and hold capacitance.
- The hold time is around 100 ps. It is limited by the settling time of the switch after the closure, and by the finite clock transition time at the end of the Hold period.
- Evaluation of the clock square wave signal generated inside the chip has shown a rise time and fall time of about 50 ps and 52ps.
- Input VSWR never exceeds 1.25 (S11 < -19 dB) over the whole input band.
- Insertion loss is 2 dB. This corresponds to a voltage gain of 0.8, and requires that the thresholds of the quantizer must be reduced appropriately. Most of the insertion loss is due to voltage division between the buffer output impedance and the output load. If the digitizer input impedance is increased, the insertion loss is reduced to 0.5 dB (voltage gain of 0.95).
- The bandwidth has a roll-off of 1 dB from 2 to 4 GHz. This is more than the 0.5 dB specification.
- The frequency response of the output buffer is flat up to 20 GHz

7FUTURE WORK

The circuit has been sent to the foundry for manufacturing, and will be available in Spring 2002. In the meantime, a test procedure will be studied to accurately characterize the performances both of the whole circuit and of the individual component blocks. In order to better evaluate individual block performances and possible problems, a second chip containing a buffer, a clock generator and two sample switch with different hold capacities has been designed. Tests will be performed at the University of Florence and at the Microelectronics department of the University of Rome - Tor Vergata.

Following tests a second, and possibly definitive version for the chip will be designed and fabricated. A mounting fixture to accommodate both the sampler, the digitizer and any auxiliary discrete circuits will be studied, to integrate the whole digitizer module in a single self-contained unit.

Cost for prototyping in the ED02AH GaAs process is 66 Euro/mm^2 per chip. Production cost for a small production series is about halved, that is 50 Euro for a 1.5 mm^2 chip.

8CONCLUSIONS

A single chip sample and hold circuit for radio astronomy applications has been designed, following the requirements for the ALMA sampler module.

In order to ensure uniform performance of the different block of the circuit (Sampler, clock generator and input/output buffer) all of them have been implemented on the same chip.

Computer simulation on the design shows that the sampler fulfills the required specifications for the ALMA sampler subsystem.

The chip is currently being fabricated, and will be tested in laboratory in spring 2001.

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